Ralph J. Pasquinelli/ Brian Chase Original 12/9/91

Linac Low Level RF (LLRF)
Operating Procedure.
8/31/94

Introduction

This note was prepared to act as a guide line for operation of the LLRF for the Linac upgrade. The new portion of the linac will operate at 805 MHz. Two stations are required for matching the beam from the 201 MHz drift tube linac cavities to the new 805 MHz side coupled cavities and are called transition 0 or Buncher and transition V or Vernier. Seven stations provide the acceleration to 400 MeV and one debuncher station located in the booster accelerator. There will be two hot spare stations: a 200 KWatt and 12 MWatt for quick replacement. Appendix I is a complete set of system block diagrams.

This procedure was written while tuning up the final version of the LLRF system. All names Lx#### are linac data base names on the Macintosh console. (For work on ACNET, the data base names are L:Lx####.) The second letter of the data base name indicates station location. Each Linac station will have a different unique character in this position of the data base name (0,V,1,2,3,4,5,6,7,D). See appendix II for complete listing of data base names used for the LLRF. Any RF voltage measurements were made with a Tektronix 7104 scope with 1 GHz bandwidth plug-ins or the HP 8990A peak power analyzer.

The cards should be plugged into the VXI crate as shown in Figure 1. NEVER PLUG/UNPLUG MODULES WITH THE VXI CRATE POWER ON. The LLRF card, the VCXO card, and the Phase Detector/Shifter cards have dip switches on the side. It is important, especially in the transition section, to see that these are properly set. Appendix III shows the proper settings. Make sure that all cards are firmly seated in the VXI crate. Do a complete inspection of the parameters in the data base before hooking up the drive cable to the solid state amplifier and fanback cable from the cavity. (Check that all settings and readings are functional.) The slot zero controller card requires a TTL trigger for T0 and a 10 MHz TTL recovered Tevatron clock. These signals are available from the control system and are plugged into the front panel of the slot zero controller. The LLRF card requires a TTL active high beam present signal from the control system for feed forward operation. The LLRF module also receives a TTL enable (active high) from the interlock system. A complete set of schematics of all VXI modules and beam loading test box are in Appendix IV. Appendix V contains the calibrations for LLRF modules and test point cables at each station. This note is not intended to have modulator operating procedure. It is assumed that the modulator is already up and running. If there are any problems or questions with the modulator refer to a qualified modulator specialist.

VXI CRATE

0	1	2	3	4	5	6	7	8	9	10	11	12
SLOT 0 CRATE CONTROLLER	VME COMPUTER LLRF	VME VERTICAL INTERCONNECT	MEMORY CARD	SPARE SLOT	360 DEG PHASE SHIFTER/DETECTOR	LOW LEVEL RF	TEMP LOOP PH DET/START UP VCXO	SPARE SLOT	SPARE SLOT	SPARE SLOT	SPARE SLOT	SPARE SLOT

Accelerating/Debuncher

0	1	2	3	4	5	6	7	8	9	10	11	12
SLOT 0 CRATE CONTROLLER	VME COMPUTER LLRF	VME VERTICAL INTERCONNECT	MEMORY CARD	SPARE SLOT	360 DEG PHASE SHIFTER/DETECTOR	LOW LEVEL RF	TEMP LOOP PH DET/START UP VCXO	360 DEG PHASE SHIFTER/DETECTOR	LOW LEVEL RF	TEMP LOOP PH DET/START UP VCXO	SPARE SLOT	SPARE SLOT

Transition

Module Description

Slot Zero Controller is the manager for the rest of the crate. It is responsible for distributing the sync clock and trigger.

VME computer does the communications and control of the RF system. It also has the task of computing the feed forward algorithm.

VME Vertical Interconnect is the serial interface to the Linac Control system.

The memory card contains the operational code and stores the default start up parameters.

The 805 Mhz Phase Detector/Shifter VXI Module provides three functions for the Linac Upgrade LLRF system. It's main purpose is to place a stable 360 phase shifter in line with the RF reference, before the LLRF controller module. This function was requested to aid in cavity phase tuning. The second function is a 360 degree phase detector. This detects the relative phase between the RF reference and the cavity fanback signal. There is also a single channel diode detector(LxSDET) that is used to monitor the cavity fanback gradient voltage(CxGRAD). The phase detector output is two signals, the in phase(I) and quadrature(Q) components. All signals are sampled at time=LLRF trigger + LxSDLY. For phase stability, the RF components of the detector and shifter are located in a temperature controlled oven(LxSTMP). This oven regulates at 50 C and should be allowed to warm up for 30 minutes for best phase stability. See appendix VI for memory map details.

Low Level RF provides the independent Amplitude and Phase closed loop control as well as the ADC's and DAC's for the feed forward loop.

Temperature Loop Phase Detector/ Start Up VCXO has a phase detector that compares the fanback to cavity drive phase (LxWGPH). This signal is used in conjunction with the VCXO portion to keep the cavity on resonance.

Cavity Temperature Control

There is a sophisticated water temperature control system for regulating the temperature of the cavities. This system is responsible for keeping the cavities at the proper resonant frequency. If the RF ceases to pulse for even a very short period of time (seconds), the resonant frequency of the cavity changes due to lack of RF heating of the cavity nose cones. When the frequency of the cavity changes even a small amount, it changes the load impedance that the klystron sees. This condition may produce excessive reflected power resulting in tripping off the klystron. The longer the klystron is off, the farther the drift in frequency. The water system cannot adjust for this small temperature change due to the long temperature time constant of the cavity. A phase detector in the VCXO card provides an error signal (LxWGPH) to this control system. It is the phase difference between the cavity drive signal and the fan back sum. Because of the high Q of the cavities, this is a very sensitive indicator of temperature change. When the error signal is out of range (as determined by the control computer) the control system switches to the local VCXO (LxVCXO and a red LED on front panel of VCXO VXI module). The local VCXO is driven by this error signal (via the computer) to the new cavity resonant frequency hence allowing the klystron to operate. As the nose cones heat up, the cavities get closer to the reference oscillator frequency. Once the error voltage (LxWGPH) is back within limits, the control is switched back to the reference oscillator (LxVCXO and a green light on the front panel of the VCXO VXI module). **If the water system is not functioning properly, it will be impossible to continue with this setup procedure.** Refer to a qualified water system expert.

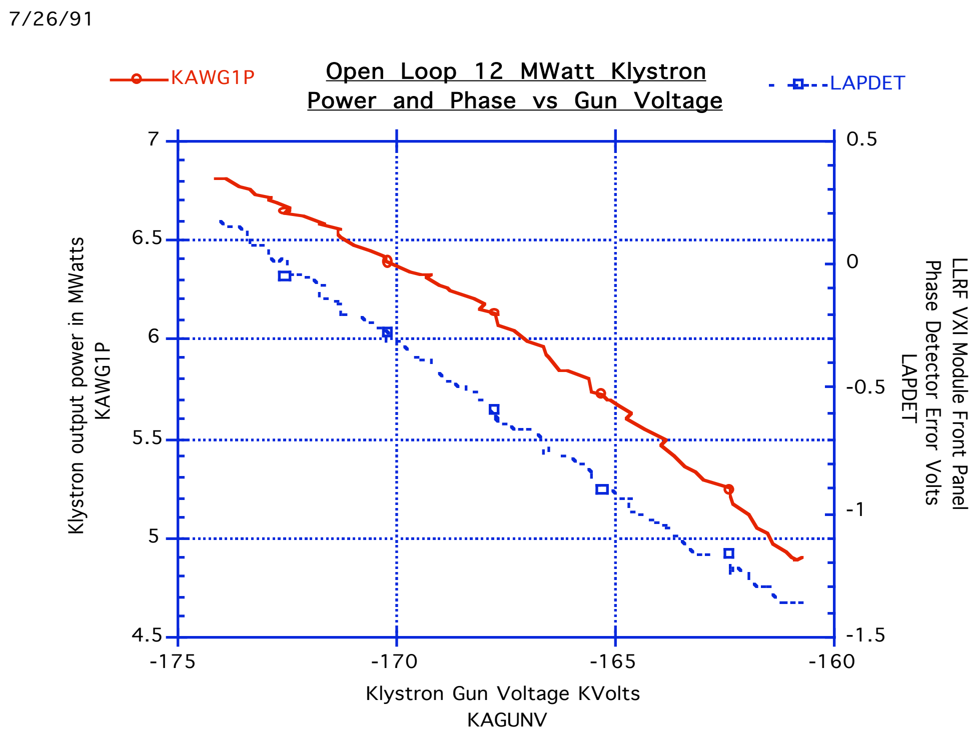


Figure 2

Parameter setup

Before setting up the parameters, it is important that the Klystron is running at its final Gun Voltage. Figure 2 is a plot of Phase Detector monitor and Klystron power versus Gun volts. Group delay variation occurs in the klystron due to kinetic energy change (gun voltage) in the tube's electron beam. Likewise the gain of the klystron changes with Gun Volts. The solid state drivers exhibit gain variation unit to unit of plus or minus 2 dB and have been internally modified to have the same phase delay. This facilitates spare replacement.

It is important to first check the power level of the master reference oscillator. The normal cabling of the reference oscillator is to the Phase Detector/Shifter card, then to the VCXO card and finally to the LLRF card by using 0.141 semi-rigid coaxes. Using a power meter verify that the level is +16 dBm +/- 0.5 dB at the input to the Phase Detector/Shifter card. If it is not, then adjust the level by using an SMA attenuator. (Available in 1 dB increments and phase matched to 3 electrical degrees at 805 MHz)

Set the length of the desired linac pulse duration by adjusting LxTDLY. Duration is nominally 60 microseconds to reduce cavity sparking. (This parameter can be as long as 200 microseconds but the modulator is limited to 125 microseconds maximum.) The FIFO memory length (LxFIFO) should be set approximately 10 microseconds longer than LxTDLY. LxFIFO is the memory depth of the feed-forward playback. This longer time can be used to provide a soft turn off function.

Adjust the magnitude set point DAC (LxGSET) to 0 volts. Make sure that the system is in open loop mode (LxMGEN, LxPHEN, LxFDFW off). Turn on the solid state driver and slowly bring up the set point DAC (LxGSET) to 3 volts. Adjustment of the drive level by means of a SMA pad at the LLRF card drive output should be made to run the system near 7.5 MWatts for an accelerating station or 120 KWatts for the transition and debuncher stations. (Observed on the directional coupler #1,#2, #3, and fanback sum forward power, calibrations are posted). For proper system gain, it is important that the fanback level to the LLRF module be set to +19 dBm. The nominal coupling value to the LLRF fanback front panel monitor is 17.25 dB plus 1 dB for the cable to the scope, i.e. +0.75 dBm or 345 mVolts zero to peak. Install a SMA attenuator at the input to the LLRF module to get this value. Figure 3 is a typical LLRF module detector transfer function that can be used as a cross check. In the same manner, set the fanback power levels to the VCXO module to +16 dBm and Phase Detector/Shifter module to +14 dBm.

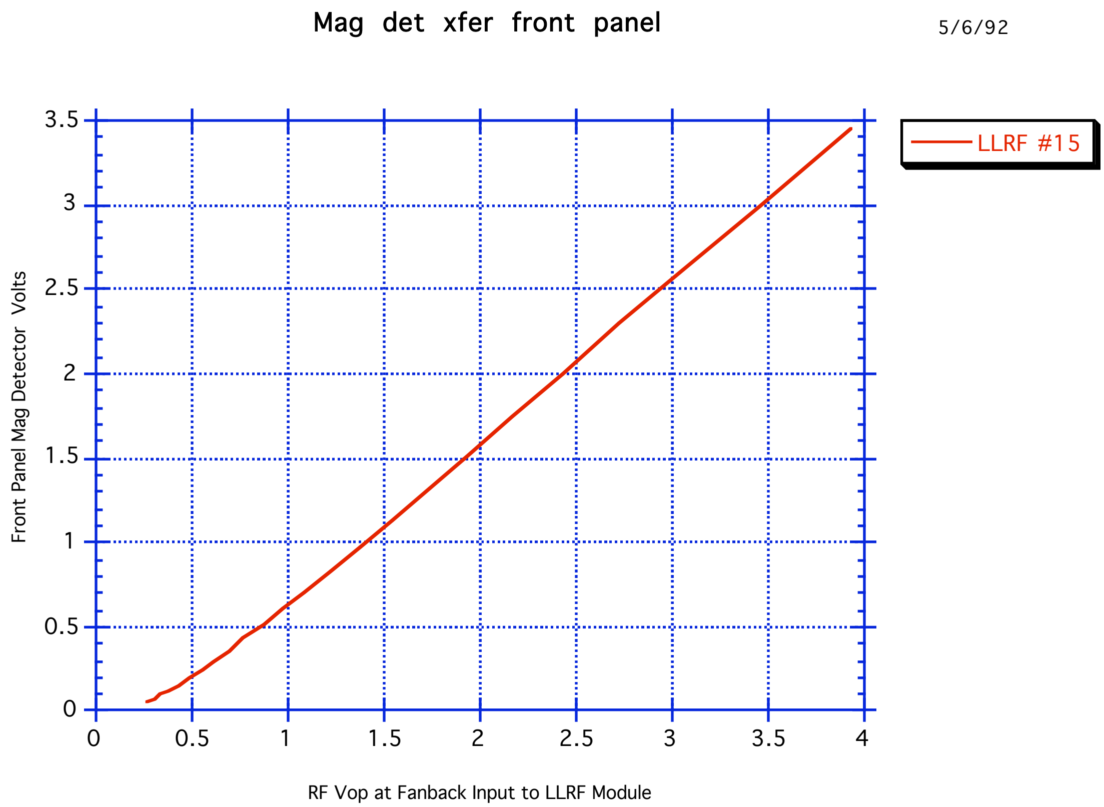


Figure 3

Setting Up Closed Loops

The LLRF module is capable of a max. drive of typically +2 dBm. The Klystron is capable of 12 MWatts output (200 KWatts transition and debuncher). It is desirable to attain 12 MWatts (or 200K Watts) with 3 dB of LLRF drive overhead. Due to reflected power trips, it may be necessary to shorten the length of the pulse (LxFIFO) to do this test. The drive monitor port on the LLRF card is 10 dB down from the drive out port. An 8-10 nanosecond test cable to the scope has approximately 1 dB insertion loss at 805 MHz. If 12 MWatts is desired with -1 dBm of drive, this will be -12 dBm at the scope or 80 mVolts zero-peak.

The following procedure is for experts only. It is written here for completeness. Two adjustment potentiometers are accessible through the side panel of the LLRF module. (The VCXO card needs to be removed to access the pots.) Trim pot R72 is the nonlinear gain control . Note that this adjustment must be made open loop (LxMGEN, LxPHEN, LxFDFW off). The intent of this adjustment is to linearize the gain of the system. Adjust LxGSET to change in 0.2 volt increments on the Macintosh console. Adjust R72 until linear steps in gain are noted on one of the forward power couplers over a range of 3 to 10 MWatts (40 to 140 KWatts). Turn down LxGSET and turn on the magnitude feedback LxMGEN. Trim pot R108 is the max. drive clamp control. It is to be adjusted to start clamping between 11 and 12 MWatts (180-200 KWatts). Typical curves from both the Varian TV klystron and the 12 MWatt Litton klystron are shown in figure 5. Note that beyond a certain drive level the gain becomes very nonlinear an could cause unstable operation. Run the system at 7.5 MWatts (120 KWatts) by increasing LxGSET and note the initial drive over shoot of the solid state forward power monitor on the scope (available on the patch panel at the top of the rack). Adjust trim pot R108 until the over shoot is approximately twice the voltage required for steady state drive level on the scope or +3dB on the power analyzer as in figure 4.

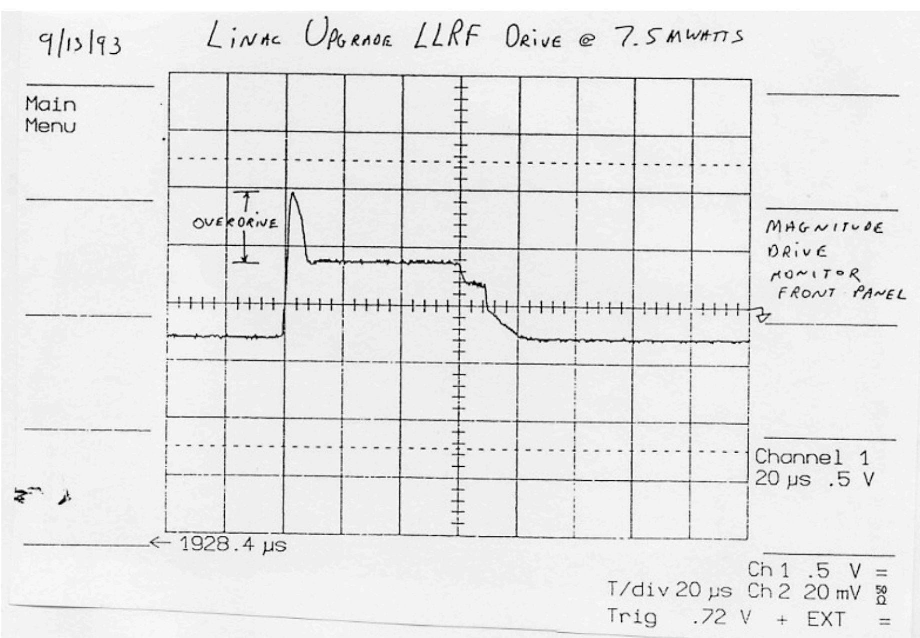


Figure 4

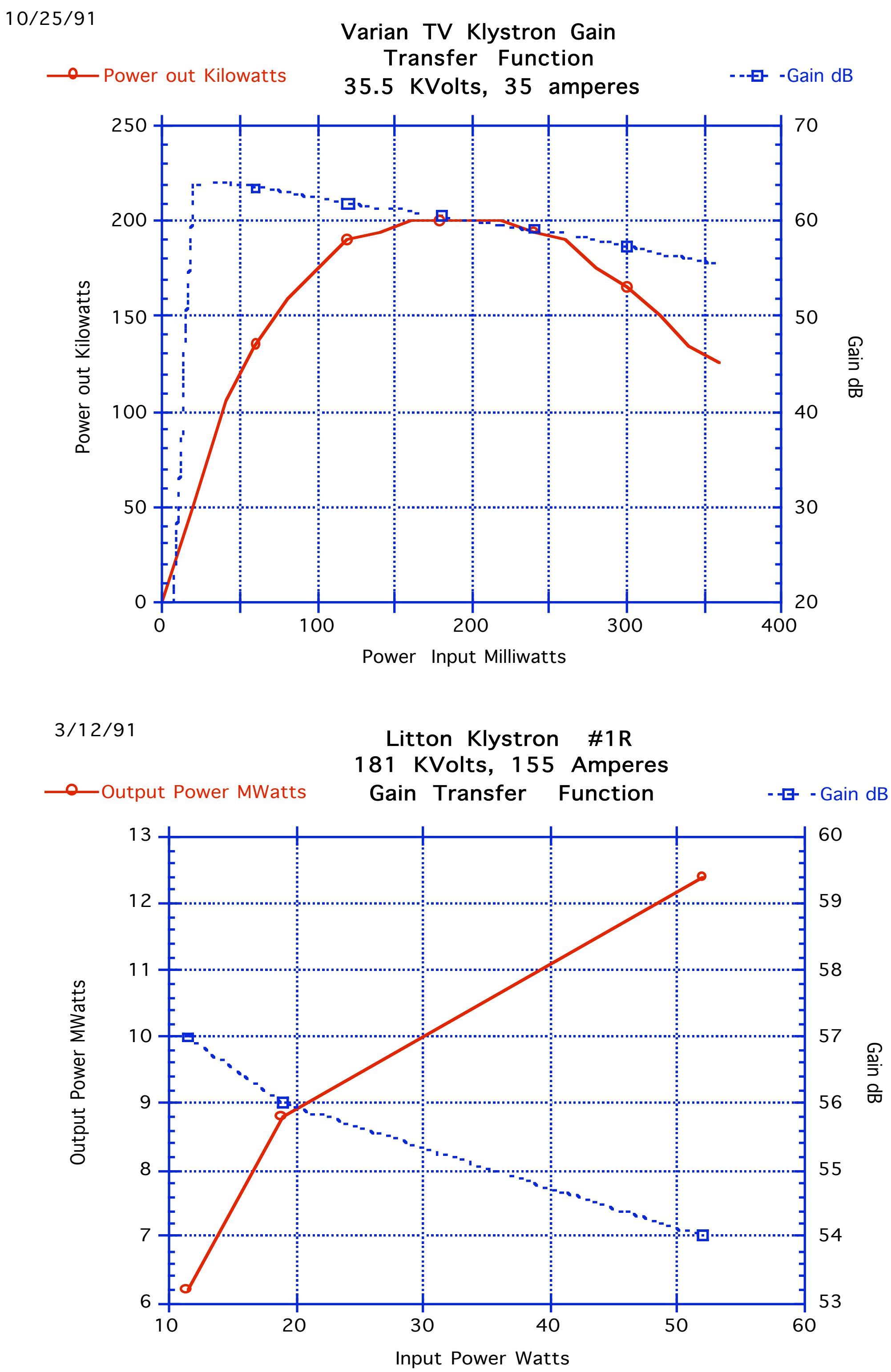

10/25/91
Varian TV Klystron Gain
Transfer Function
35.5 KVolts, 35 amperes
Power out Kilowatts
Gain dB
Power out Kilowatts
Gain dB
250
200
150
100
50
0
70
60
50
40
30
20
0
100
200
300
400
Power Input Milliwatts
3/12/91
Litton Klystron #1R
181 KVolts, 155 Amperes
Gain Transfer Function
Output Power MWatts
Gain dB
Output Power MWatts
Gain dB
13
12
11
10
9
8
7
6
60
59
58
57
56
55
54
53
10
20
30
40
50
60
Input Power Watts

Figure 5

For stable operation, it is important to operate the phase shifter in the LLRF module at the correct voltage. These phase shifters are nonlinear devices. Stable gain is achieved when they are operated in the 20 to 30 degrees per volt range (Figure 6), nominally 4-6 volts on the phase shifter control voltage input. Set the open loop phase set DAC to 5 volts (LxPOPN). Close the phase loop (LxPHEN on) and the phase detector signal on the monitor should appear close to zero volts as it does in figure 7 (indication of phase regulation). If the results are not similar to those in figure 7, there is a possibility that the sign of the feedback could be wrong so change (LxPHSN). The nominal operating setting for LxPHSN should be zero. When a klystron needs to be changed, the setting of LxPOPN can be adjusted to compensate for small phase changes (20-50 degrees) between klystrons. If the new klystron has a phase difference larger than 50 degrees, a new fanback sum cable may have to be cut.

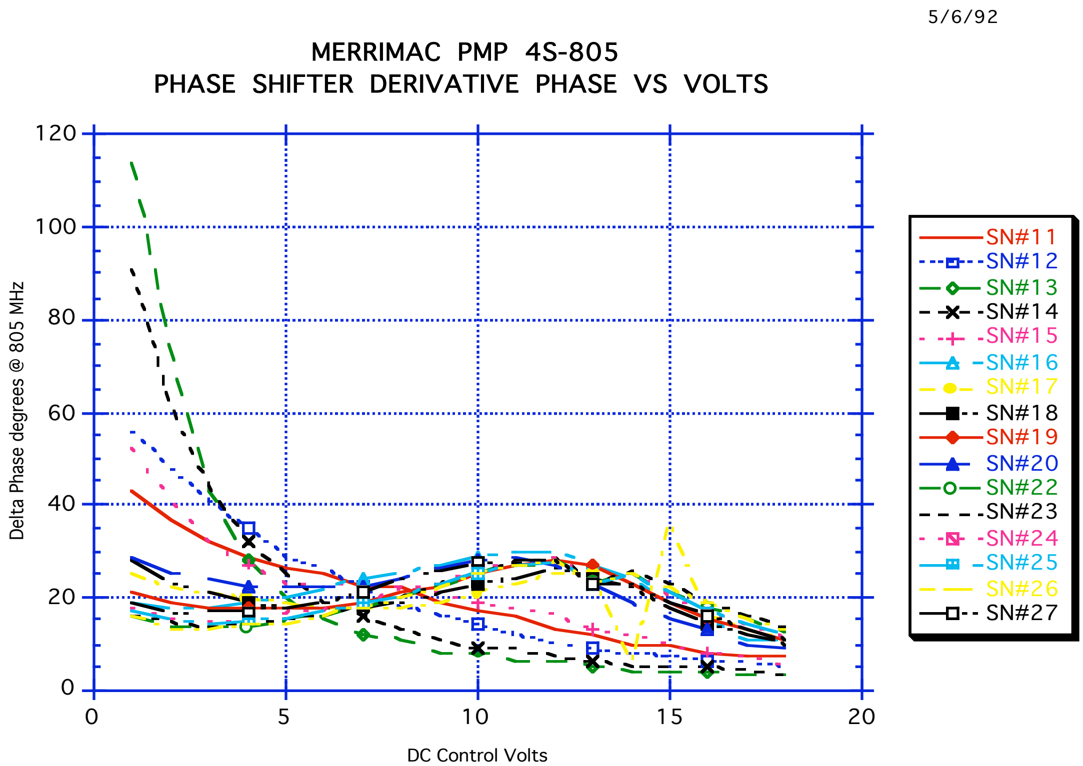


Figure 6

Feed-Forward.

To initially test the feed-forward functions (no beam available), first connect the beam load test box in series with the LLRF module output and the solid state driver input. (This box introduces a magnitude and phase step during the linac pulse to simulate beam loading on the cavity. Actual beam loading performance will not be observable unless there is beam in the linac.) The T0 trigger is necessary for triggering the test box. With all loops in open loop mode (LxMGEN, LxPHEN, LxFDFW off) adjust the beam load box for a 18 degree phase step and a 10 percent amplitude step. These values have been projected as the worst case system beam loading.

Adjustment can be made using the pots that are recessed in the front panel of the beam load test box. The calibration for the phase detector front panel on the LLRF module is approximately 30 millivolts per degree and dependent on fanback power level, see figure 8. The front panel phase shifter monitor in the beam load box should be operating at approximately 4 to 5 volts. Monitor the magnitude detector on the LLRF for a 10 percent dip as in figure 9. Turn on the feedback loops (LxMGEN, LxPHEN on) and notice that they correct some of the step discontinuity but not all, see figure 10. Maximum stable gain prohibits better performance hence the requirement of feed-forward.

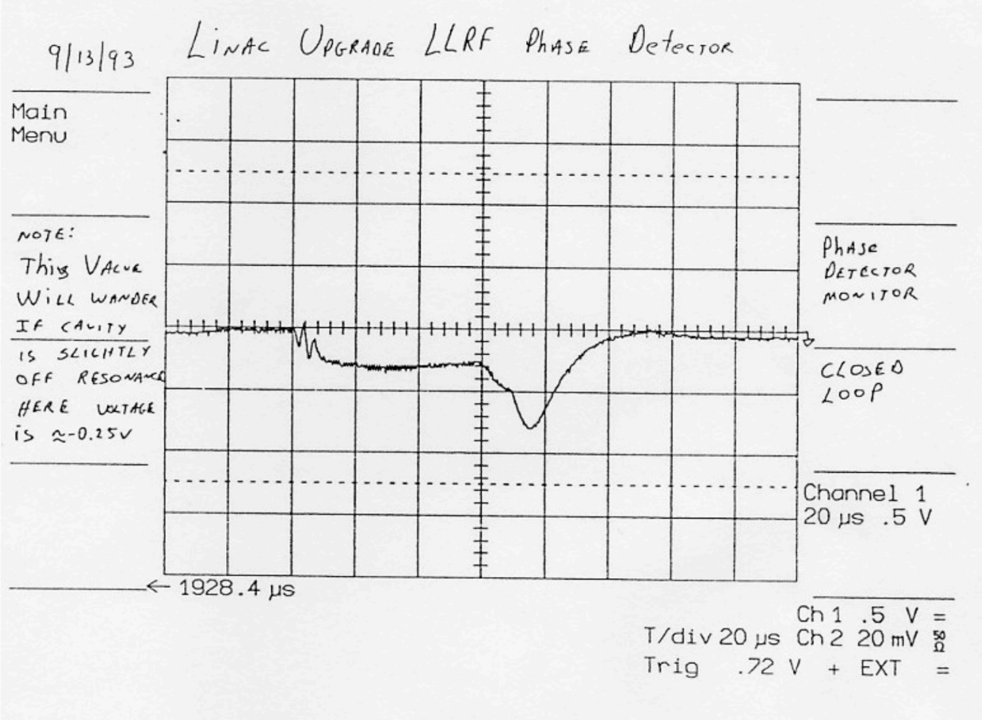


Figure 7

There is a front panel input on the LLRF module for a TTL active high beam present signal. This can be monitored from the control system via LxBEAM. In the final linac this signal will be generated by the control system based on beam at the first linac drift tube station. The presence of this signal tells the feed-forward computer to modify the feed-forward signal. The feed-forward wave form is modified only on machine cycles that have beam in them. Without the beam present signal, the computer will continue to play out the last computed wave form computed from beam loading.

Feed-forward Parameter Setup

Feed-forward gain (LxMGAI magnitude loop, LxPGAI phase loop) is the multiplier for the feed-forward error signal. It's value will determine the time response of the learning algorithm. The higher the gain the faster the response. Too high a value can be unstable or susceptible to noise. For LxMGAI=12 the hardware provides unity gain across the input to output of U21 on the LLRF schematic. Likewise for LxPGAI=2 provides unity gain input to output of U14. Optimum gain was calculated at LxMGAI=676 but may be unstable. A value of 340 for both loops has worked well so far.

Feed-forward offset (LxMOFF, LxPOFF) is the baseline value in DAC counts for the feed-forward signal. The DAC's are 12 bit or 4096 counts and are offset by 1/2 full scale in the analog circuit. A value of 2048 (mid-scale 2.6 volts measured) will effectively be 0 volts out of the fast DAC for the feed-forward network. Offset gain was measured to be 1.27 mV/count. The time constant for the feed forward loops was measured to be 24 clock cycles.

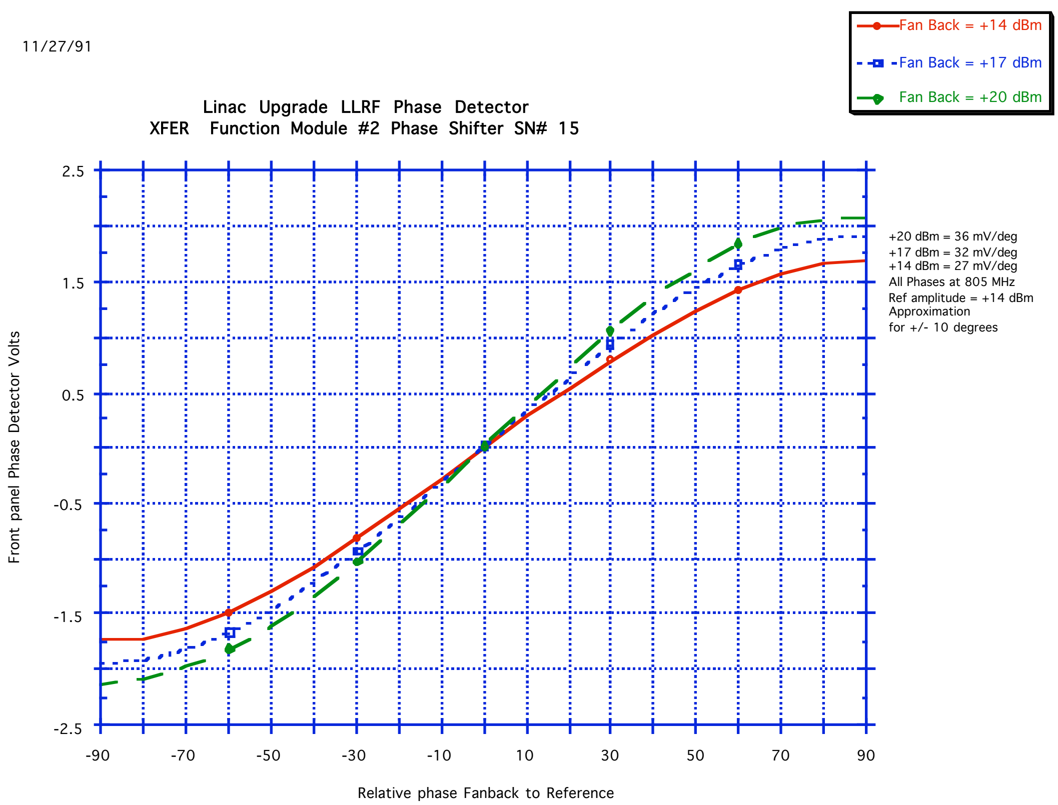


Figure 8

Feed-Forward Timing Setup

Use a digital scope to measure the start and stop times of the beam loading signal as seen on the LLRF module front panel phase detector and the magnitude detector. The scope trigger must be the system trigger T0. Refer to figure 11 for proper timing. LxPHNO, LxMNO, LxPHN1, LxMN1, LxPHN2, and LxMN2 are all "duration times" with respect to LxxxTx. Set the no beam loading sample start times to a stable point before the beam load.

Turn on the feed-forward loops with LxFDFW. When the times are properly set performance similar to Figure 12 should be visible. Figure 12 shows better than 1 percent amplitude and 1 degree phase regulation through out the beam loading pulse. Slight adjustments of LxPHT2 and LxMT2 will improve the initial transient response.

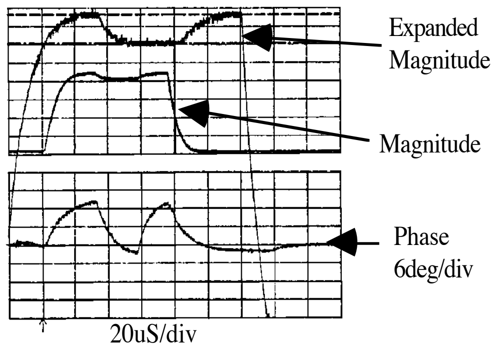


Figure 9. System open loop response to simulated 7.5% beam loading and 18 deg. phase shift. Klystron operating at 7.5 Mwatts,

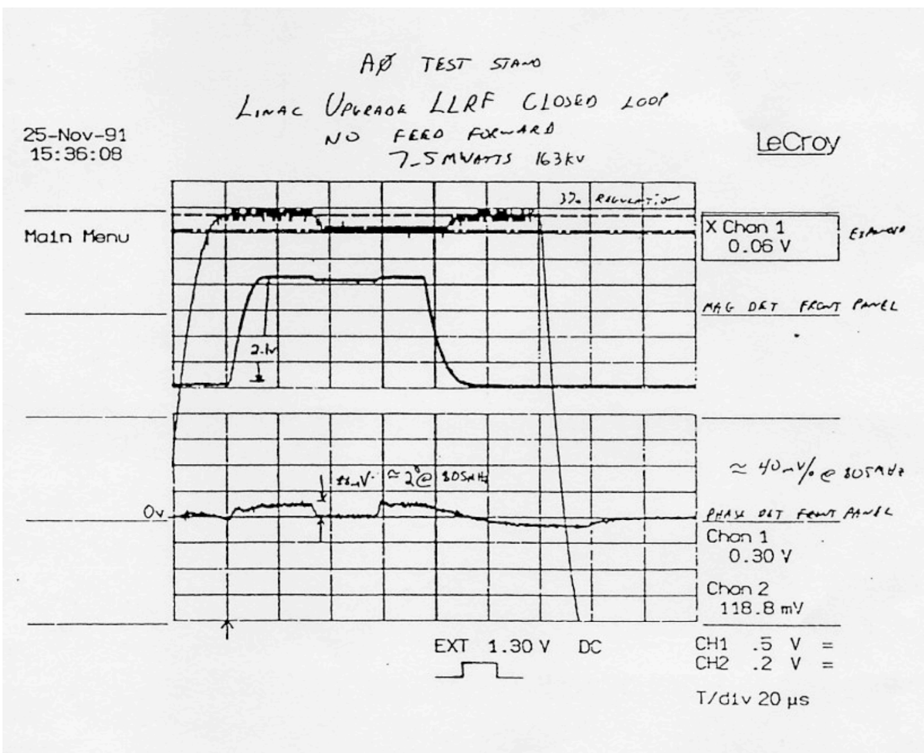


Figure 10

LLRF DATA BASE FOR LINAC TIME LINE

RJP 7/1/91
Modified
2/22/93

T0...START TIME
LZPHT0..PHASE NO LOAD SAMPLE START TIME
LZPHNO..PHASE NO LOAD SAMPLE DURATION TIME
LZMT0..MAGNITUDE NO LOAD SAMPLE START TIME
LZMN0..MAGNITUDE NO LOAD SAMPLE DURATION TIME
LZPHT2..PHASE FFWD PLAYBACK START TIME
LZMT2..MAGNITUDE FFWD PLAYBACK START TIME
LZPHT1..PHASE BEAM LOAD SAMPLE START TIME
LZPHN1..PHASE BEAM LOAD SAMPLE DURATION TIME
LZMT1..MAGNITUDE BEAM LOAD SAMPLE START TIME
LZMN1..MAGNITUDE BEAM LOAD SAMPLE DURATION TIME
LZADLY...DATA AQUISITION SAMPLE TIME (VARIABLE)
LZTDLY...PULSE DURATION SET TIME
LZPHN2..PHASE FFWD PLAYBACK STOP TIME
LZMN2..MAGNITUDE FFWD PLAYBACK STOP TIME
LZFIFO...FIFO MEMORY TIME LENGTH

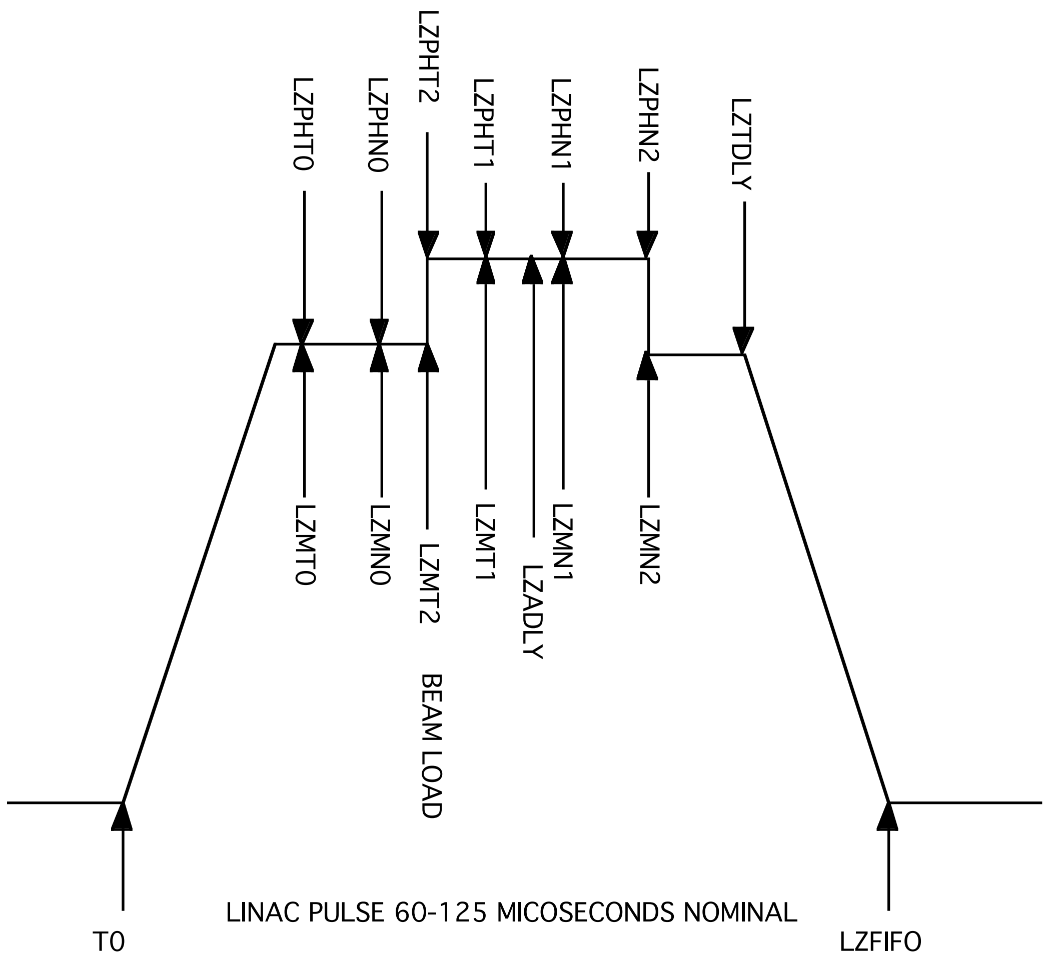


Figure 11

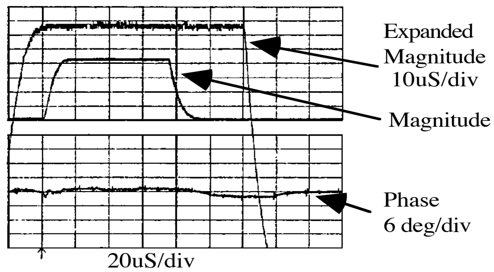


Figure 12. System response to simulated 7.5% beam loading and 18 deg. phase shift with feedback and feedforward on. Klystron is operating at 7.5 Mwatts.

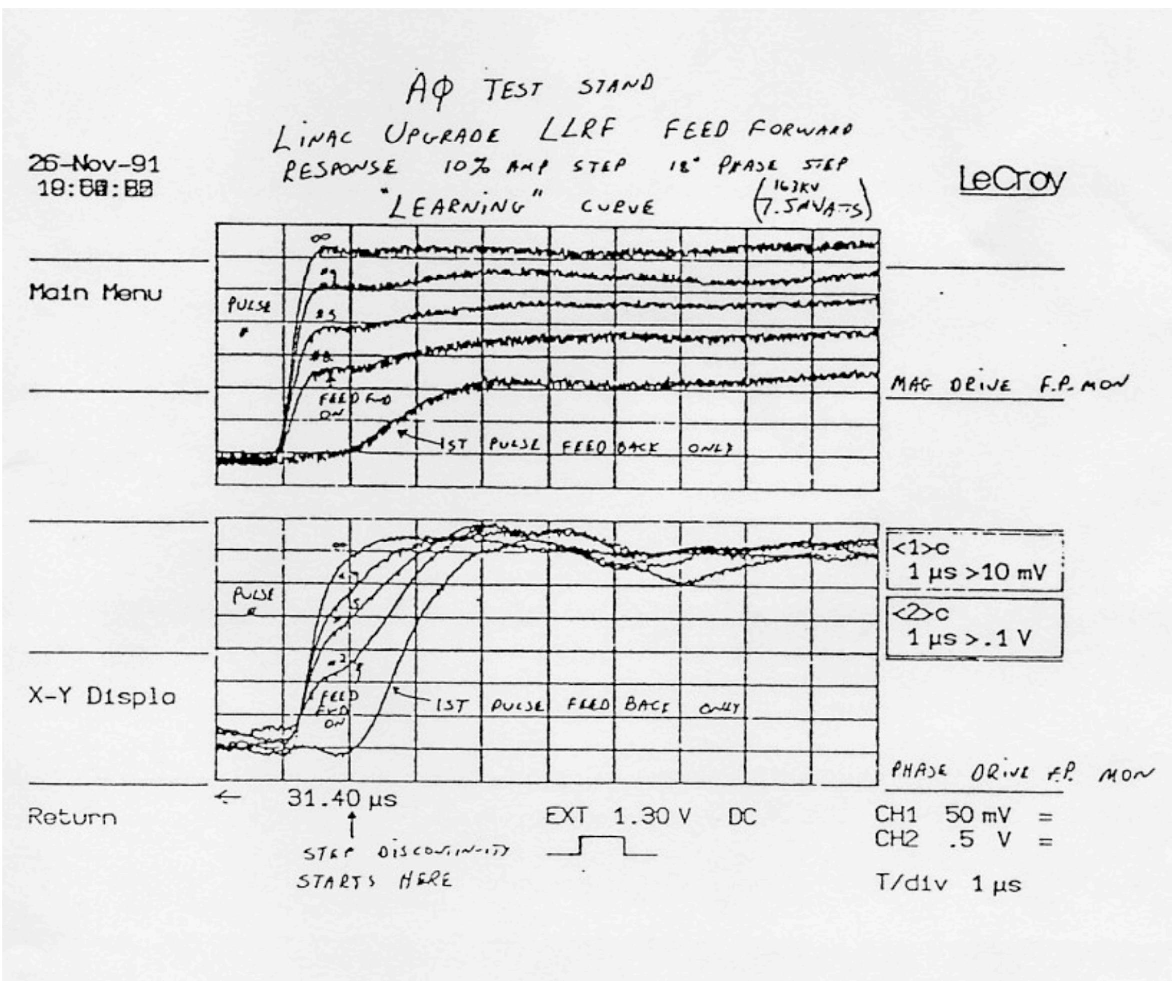


Figure 13

The feed-forward system is an adaptive system. Figure 13 shows the learning curves as viewed on the Magnitude and Phase Drive LLRF Module front panel monitors. After about 15 pulses the system achieves best performance. This is about 1 second real time with the linac operation at 15 Hz.

Figures 14 and 15 show the regulation performance versus operating point of the Magnitude and Phase loops respectively. Magnitude loop regulates over a 6 dB range and the Phase loop regulates over a 25-50 degree range. For operations, the linac amplitude will be fixed hence 6 dB is ample and phase regulation far exceeds beam loading.

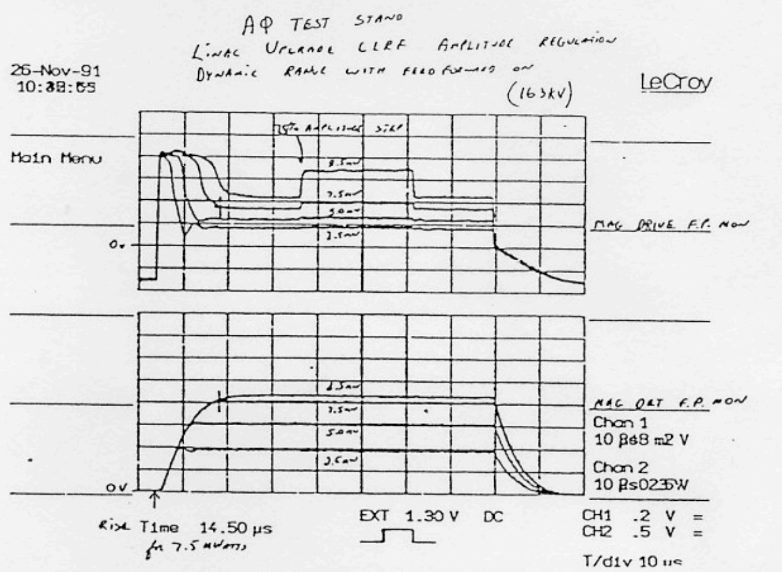


Figure 14

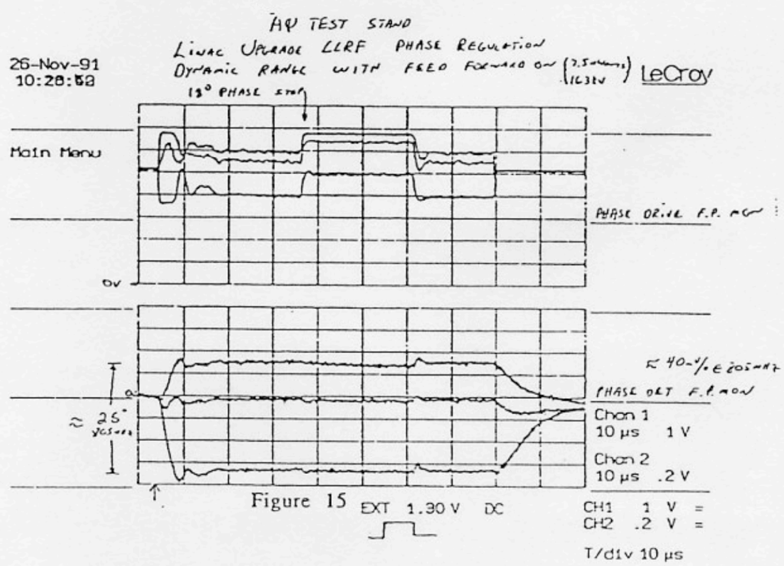
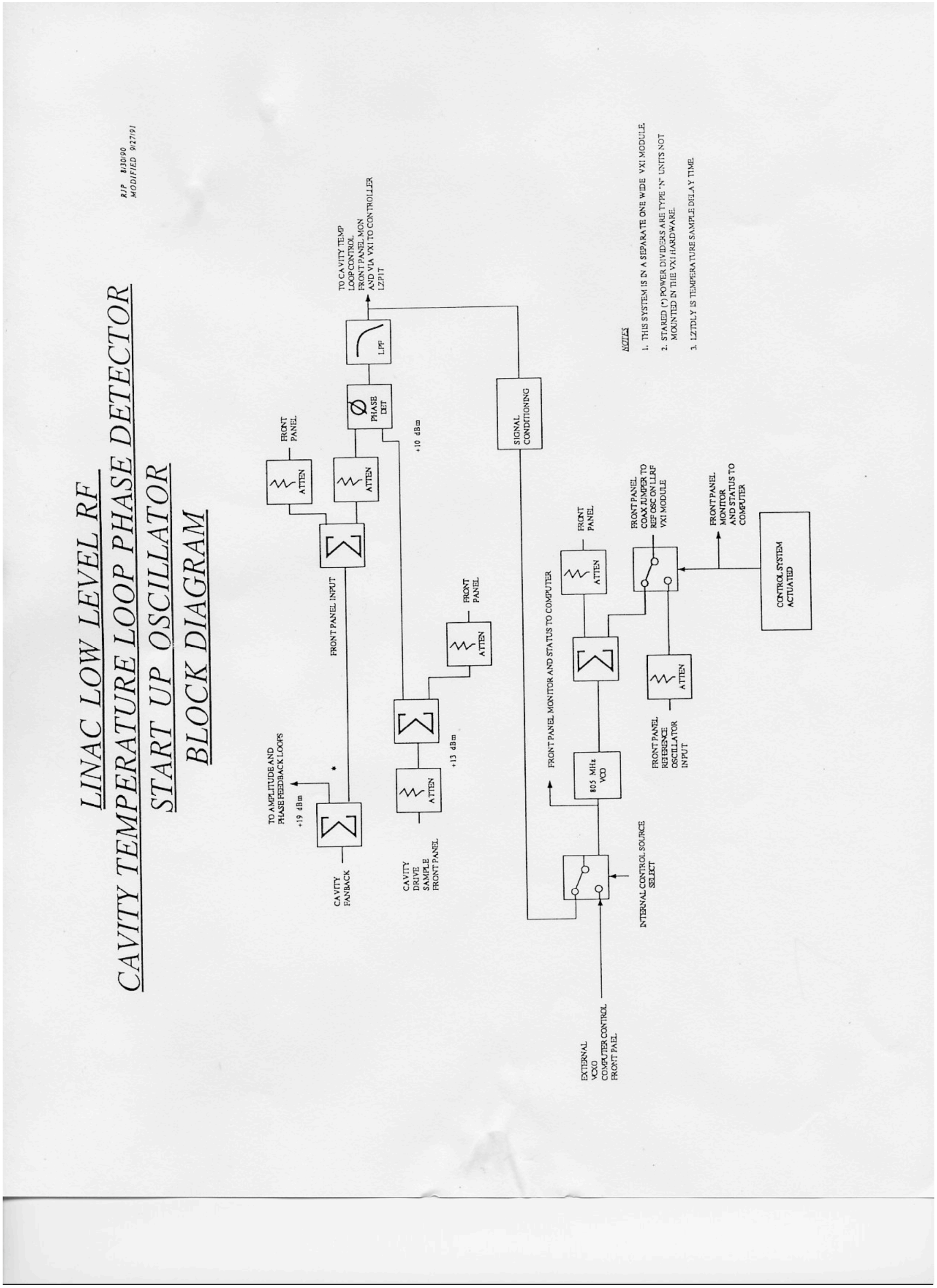
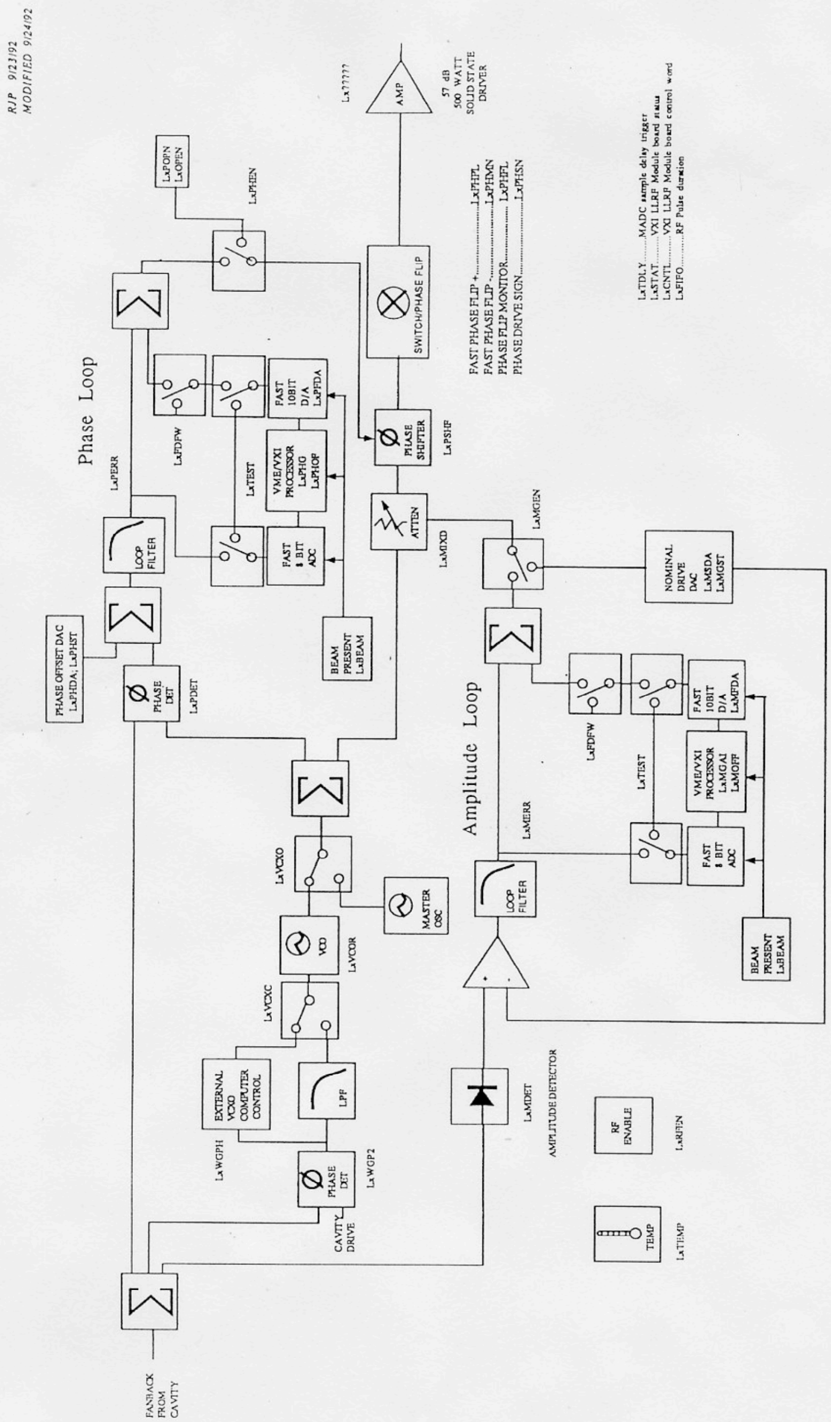


Figure 15

Appendix I: Block Diagrams

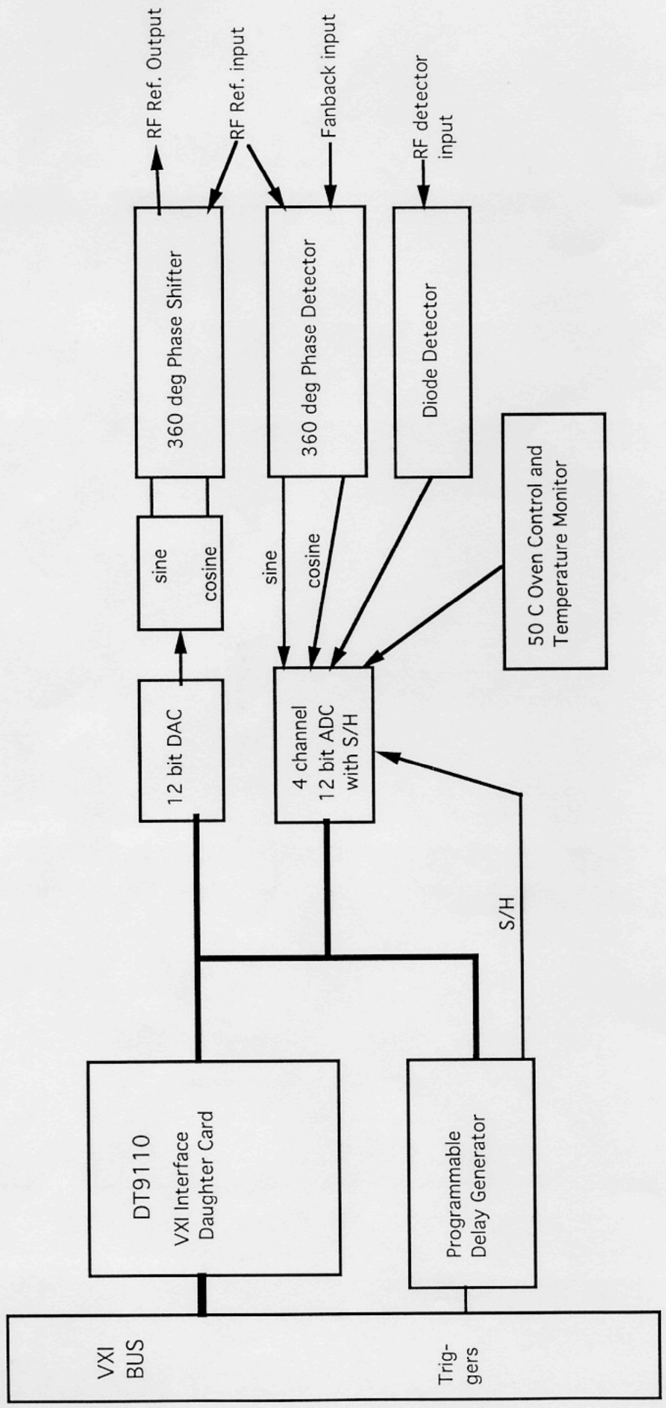

LINAC LOW LEVEL RF
CAVITY TEMPERATURE LOOP PHASE DETECTOR
START UP OSCILLATOR
BLOCK DIAGRAM
RJP 8/30/90
MODIFIED 9/27/91
CAVITY FANBACK
+19 dBm
TO AMPLITUDE AND PHASE FEEDBACK LOOPS
*
FRONT PANEL INPUT
ATTEN
FRONT PANEL
PHASE DET
+10 dBm
LPF
TO CAVITY TEMP LOOP CONTROL FRONT PANEL MON AND VIA VXI TO CONTROLLER LZPIT
CAVITY DRIVE SAMPLE FRONT PANEL
+13 dBm
SIGNAL CONDITIONING
FRONT PANEL MONITOR AND STATUS TO COMPUTER
EXTERNAL VCXO COMPUTER CONTROL FRONT PAEL
INTERNAL CONTROL SOURCE SELECT
805 MHz VCO
FRONT PANEL REFERENCE OSCILLATOR INPUT
FRONT PANEL COAX JUMPER TO REF OSC ON LLRF VXI MODULE
FRONT PANEL MONITOR AND STATUS TO COMPUTER
CONTROL SYSTEM ACTUATED
NOTES
1. THIS SYSTEM IS IN A SEPARATE ONE WIDE VXI MODULE.
2. STARED (*) POWER DIVIDERS ARE TYPE "N" UNITS NOT MOUNTED IN THE VXI HARDWARE.
3. LZTDLY IS TEMPERATURE SAMPLE DELAY TIME.

LINAC LOW LEVEL RF CONTROL DIAGRAM



BEC 7/6/93

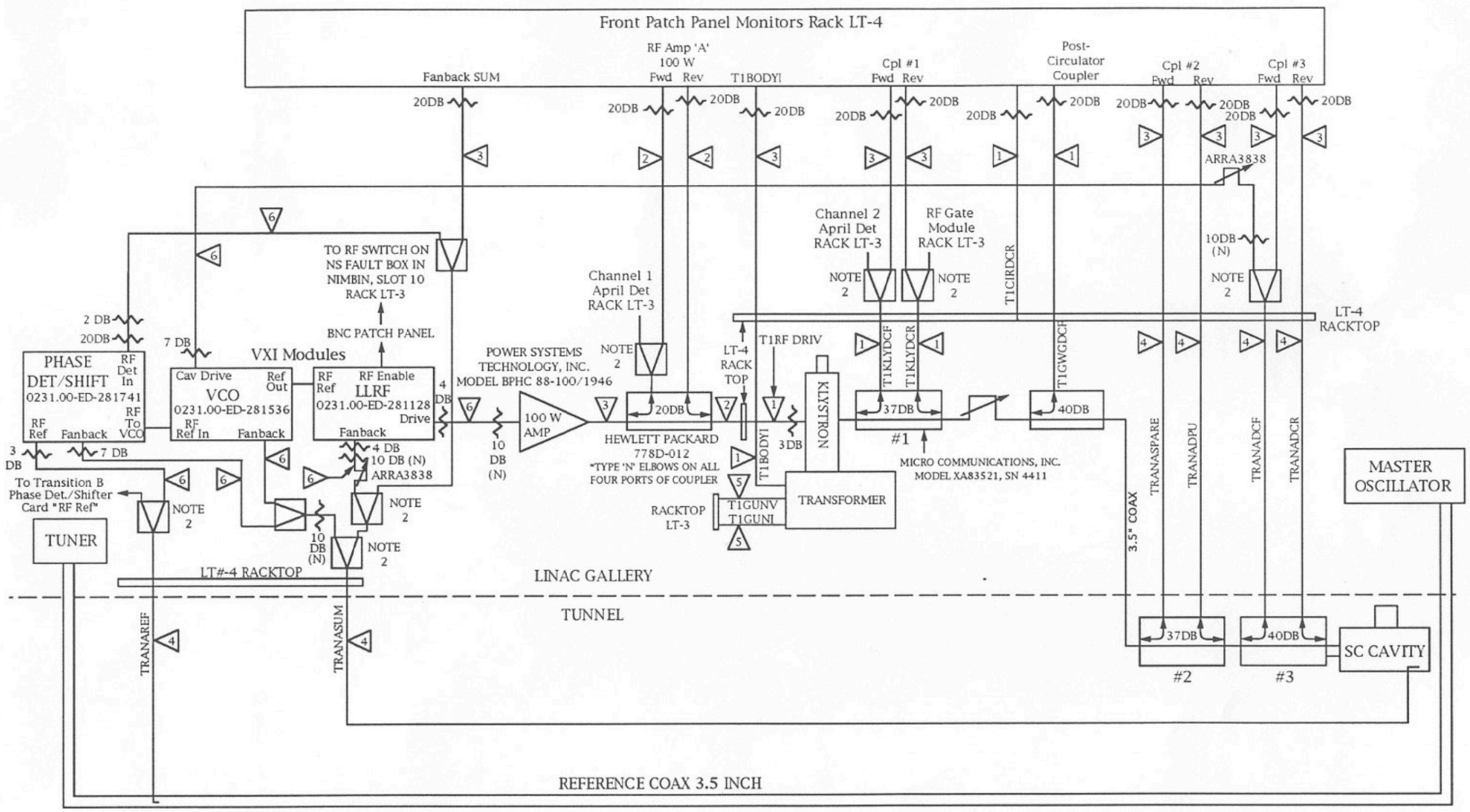
805 MHz Phase Detector/Shifter Block Diagram



LINAC UPGRADE RF CONNECTIONS

TRANSITION 'A' or '1' or 'O'

RJP 10/19/92
WJM 12/22/93



#	CABLE TYPE	LENGTH
1	3/8" ANDREWS LDF2-50	
2	1/4" ANDREWS FSJ1-50A	60" TYPICAL 5950PS
3	1/4" ANDREWS FSJ1-50A	24" TYPICAL 2362PS
4	1/2" ANDREWS LDF4-50A	
5	1/4" ANDREWS FSJ1-50A	
6	TIMES CABLE SF142B	
7		
8		
9		
10		

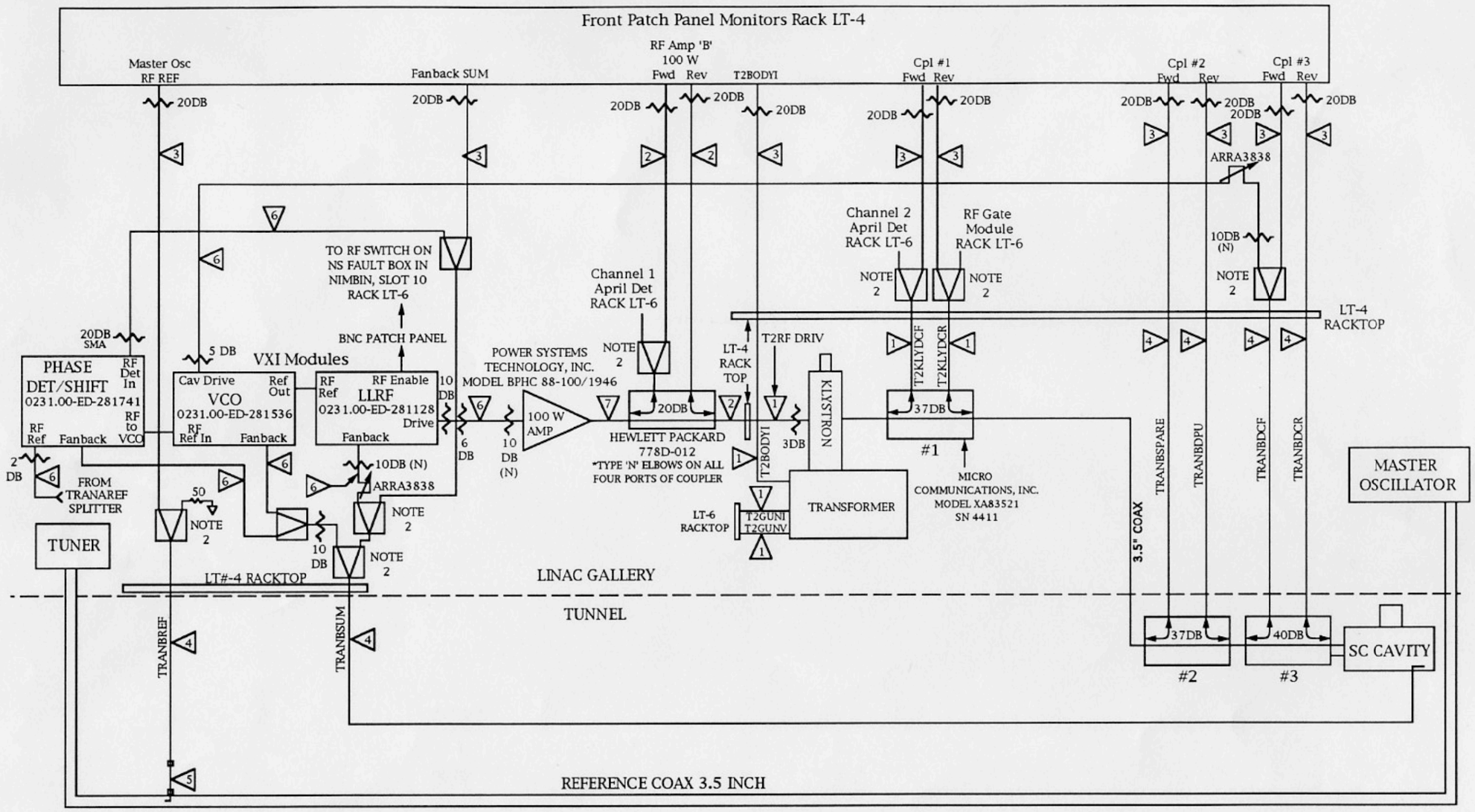
Notes

1. All 20dB Pads are Type N, by JFW uWave, Model 50F-20. Typical length is 235ps. 10DB 'N' pads are by MACOM #3082-6143-10, typical length is 195ps. All other pads are SMA type by Midwest uWave, #ATT-0294-xx-000-02 (where xx is db value), typical SMA length is 84ps.
2. All splitters are Type N installed in ceiling of Relay rack with exception of splitter mounted on directional coupler after 100W amp. All are by Merrimac uWave, 2-way model PDN-20-805/67505, 3-way model PDN-30-805/67506. 3-way typical length is 576ps (5.94DB loss @ 805Mhz), 2-way typical length is 432ps (3.54db loss @ 805Mhz).

LINAC UPGRADE RF CONNECTIONS

TRANSITION 'B' or '2' or 'V'

RJP 10/19/92
WJM 11/17/93



#	CABLE TYPE	LENGTH
1	3/8" ANDREWS LDF2-50	
2	1/4" ANDREWS FSJ1-50A	60" TYPICAL 5950PS
3	1/4" ANDREWS FSJ1-50A	24" TYPICAL 2362PS
4	1/2" ANDREWS LDF4-50A	
5	1/2" ANDREWS LDF4-50A	'B' EXTENSION 25.454NS
6	TIMES CABLE SF142B	
7	1/4" ANDREWS FSJ1-50A	30" TYPICAL 2989PS
8		
9		
10		

Notes

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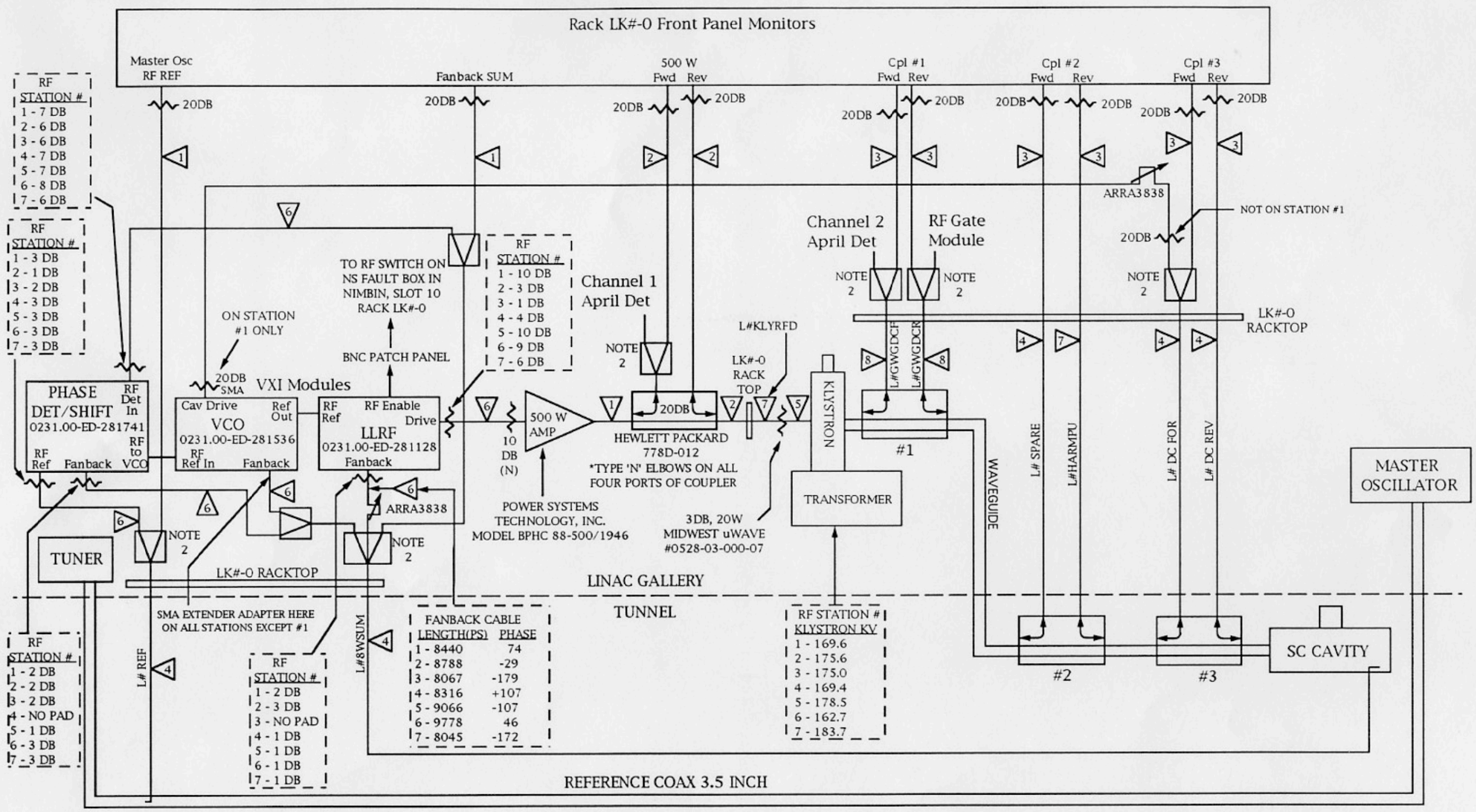
3.

LINAC UPGRADE RF CONNECTIONS

RJP 10/19/92
WJM
12/22/93



#	CABLE TYPE	LENGTH
1	1/4" ANDREWS FSJ1-50A	18" TYPICAL 1771PS
2	1/4" ANDREWS FSJ1-50A	60" TYPICAL 5950PS
3	1/4" ANDREWS FSJ1-50A	24" TYPICAL 2362PS
4	1/2" ANDREWS LDF4-50A	
5	1/2" ANDREWS FSJ4-50B	TYPICAL 2600PS
6	TIMES CABLE SF142B	
7	3/8" CABLEWAVE FCC38-50	
8	1/4" ANDREWS FSJ1-50A	
9		
10		

EACH RF STATION 1-7
HAS THIS SAME LAYOUT

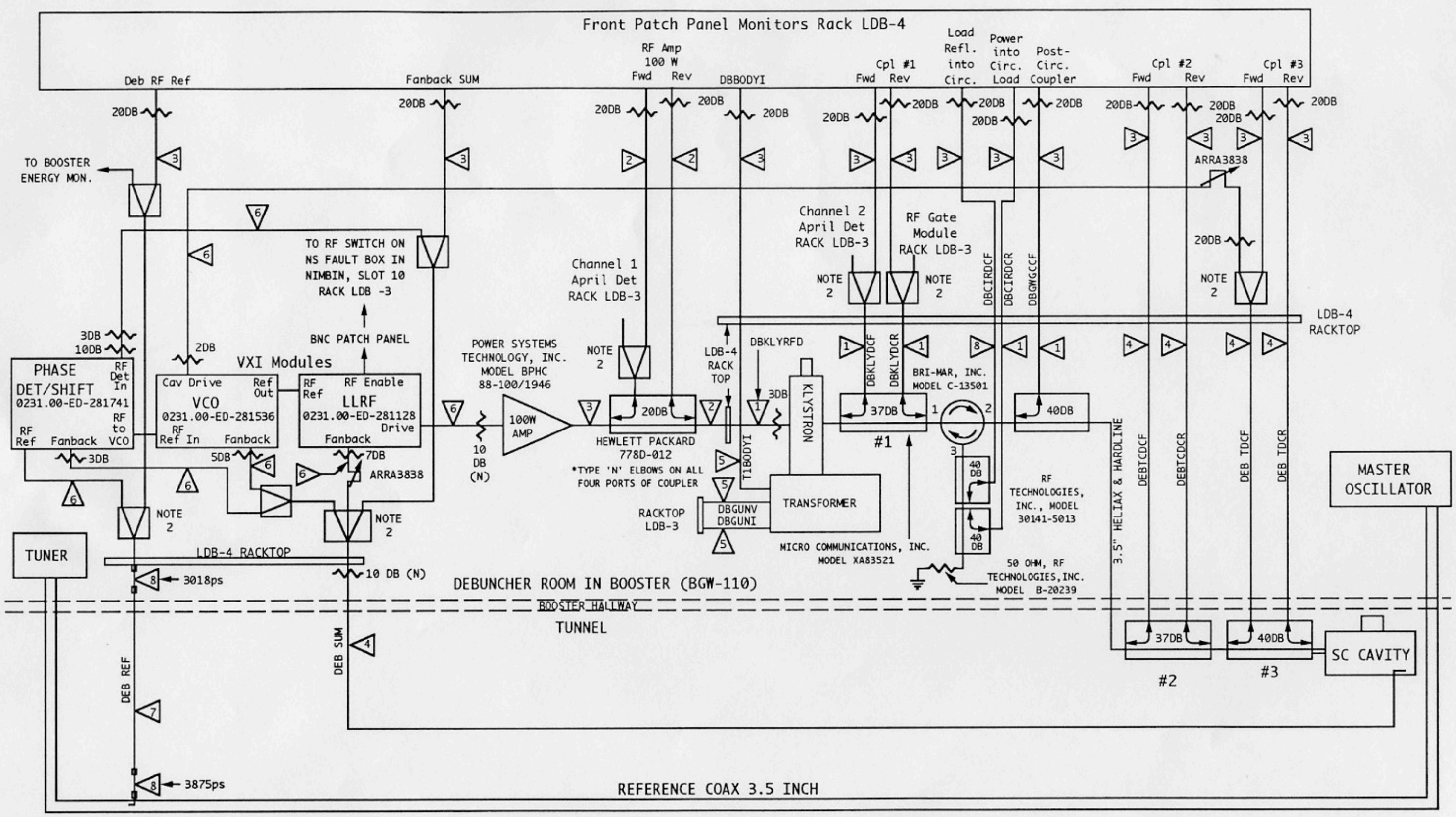
Notes

1. All 20dB Pads are Type N, by JFW uWave, Model 50F-20. Typical length is 235ps. All other pads are SMA unless stated otherwise(typical length is 84ps).
2. All splitters are Type N installed in ceiling of relay rack with exception of splitter mounted on directional coupler after 500 watt amp. All are by Merrimac uWave, 2-way model is PDN-20-805/67505, 3-way model is PDN-30-805/67506. 2-way typical length is 432ps (3.54db loss @ 805Mhz) and 3-way typical length is 576ps (5.94db loss @ 805Mhz).
3. The '#' symbol in the racktop name and cable names refer to each RF station location 1 thru 7 and their associated cables. L# DC FOR cable name would be L4 DC FOR for that cable on RF station 4, at rack LK4-0.
4.

LINAC UPGRADE RF CONNECTIONS

DEBUNCHER

RJP 10/19/92
WJM 12/24/93



#	CABLE TYPE	LENGTH
1	3/8" ANDREWS LDF2-50	
2	1/4" ANDREWS FSJ1-50A	60" TYPICAL 5950PS
3	1/4" ANDREWS FSJ1-50A	24" TYPICAL 2362PS
4	1/2" CABLEWAVE FLC12-50	
5	1/4" ANDREWS FSJ1-50A	
6	TIMES CABLE SF142B	
7	7/8" ANDREWS HJ5-50	
8	1/2" ANDREWS FSJ4-50B	
9		
10		

Notes

1. All 20dB Pads are Type N, by JFW uWave, Model 50F-20. Typical length is 235ps. Other pads are SMA, by Midwest uWave, model #ATT-0294-xx-000-02 (where xx is the db value), typical SMA length is 84 ps.
2. All splitters are Type N installed in ceiling of Relay rack with exception of splitter mounted on directional coupler after 100W amp. All are by Merrimac uWave, 2-way model PDN-20-805/67505, 3-way model PDN-30-805/67506. 3-way typical length is 576ps, 2-way typical length is 432ps.

Appendix II: Database definitions.

LLRF Module

LxADLY: MADC sample delay time from trigger. Can be used to make fast time plots.
LxBEAM: Beam present status readback. feed-forward modifies output only when this status is true.
LxCNTL: VXI LLRF module board control word.
LxFDFW: Enables/disables the feed-forward loops.
LxFIFO: Sets the time length of the RF gate pulse.
LxMDET: Magnitude loop diode detector readback.
LxMERR: Magnitude loop error voltage.
LxMFDA: Magnitude feed-forward fast playback DAC
LxMGAI: Magnitude feed-forward gain set DAC.
LxMGEN: Enables/disables the magnitude feedback loop,.
LxMGST: Magnitude closed loop set point DAC readback.
LxMIXD: Magnitude loop mixer attenuator drive voltage.
LxMN0: Magnitude feed-forward no load sample duration time.
LxMN1: Magnitude feed-forward beam load sample duration time.
LxMN2: Magnitude feed-forward playback stop time.
LxMOFF: Magnitude feed-forward offset DAC.
LxGSET: Magnitude closed loop set point DAC.
LxMT0: Magnitude feed-forward no load sample start time.
LxMT1: Magnitude feed-forward beam load sample start time.

LxMT2: Magnitude feed-forward playback start time.
LxOPEN: Phase open loop set point DAC readback.

LxPDET: Phase loop phase detector voltage.
LxPERR: Phase loop phase detector voltage.
LxPFDA: Phase feed-forward fast playback DAC.
LxPHDA: Phase closed loop set point DAC.
LxPHEN: Enables/disables the phase feedback loop.
LxPHFL: Fast drive phase flip monitor readback.
LxPHG: Phase feed-forward gain set DAC.
LxPHMN: Fast minus drive phase flip control.
LxPHN0: Phase feed-forward no load sample duration time.
LxPHN1: Phase feed-forward beam load sample duration time.
LxPHN2: Phase feed-forward playback stop time.
LxPHOF: Phase feed-forward offset DAC.
LxPHPL: Fast plus drive phase flip control.
LxPHSN: Toggles the output phase by zero or 180 degrees.
LxPHST: Phase closed loop set point DAC readback.
LxPHT0: Phase no load sample start time.
LxPHT1: Phase feed-forward beam load sample start time.
LxPHT2: Phase feed-forward playback start time.
LxPOPN: Phase open loop set point DAC.
LxPSHF: Phase loop phase shifter drive voltage.
LxRFEN: RF enable read back status.
LxRFIN RF inhibit control.
LxSTAT: VXI LLRF module board status word.

Appendix II: Database definitions continued

LLRF Module

LxTDLY: Soft turn off delay.
LxTEMP: VXI LLRF module on board temperature monitor readback.
LxTEST: This is a test mode which allows the fast DAC and ADC to talk to each other.
LxPHPT Memory plot address for phase error wave form.
LxMGPT Memory plot address for magnitude error wave form.
LxPFPT Memory plot address for phase feed forward wave form.
LxMFPT Memory plot address for magnitude feed forward wave form.
L:LxPTLT Phase Feed Forward Tilt
L:LxMTLT Magnitude Feed Forward Tilt
L:LxFLRN Feed Forward Learn

VCXO Module

LxWGPH Wave guide to cavity phase. Used to tune cavity temperature.
LxWGP2 Wave guide to cavity phase sampled at time LxADLY.
LxVCOR VCXO control voltage readback.
LxVCXC Internal or external VCXO loop control. Should read EX.
LxVCXO RF reference line or local VCXO switch control. This is controlled by the water control loops. (Jim Crisp)

Phase Detector/Shifter Module

CxPOFF I Q phase shifter offset. 0-360 degree offset to readback CxPHAS
CxPHAS 0-360 degree readback of I Q components from phase detector
LxSDLY Sample time delay from LLRF trigger.
CxPADJ Phase Shifter set DAC
LxSIPH Voltage of in phase port of phase detector.
LxSQPH Voltage of quadrature phase port of phase detector.
LxSDET Voltage of diode detector.
LxSTMP Temperature of RF oven. (Should be 50 C).

Cavity Power

KxPOWR Cavity fanback power.
LxRFGV Cavity gradient voltage.
CxGRAD Cavity gradient normalized to one.

ADDENDUM To Appendix II. (1/6/94)

Gradient Regulation Loop For Linac Upgrade Klystron Stations

The program is a "Local Application" which requires 4 local (changeable) parameters and two startup parameters:

KxWAIT Essentially, the number read from this parameter tells the program how long to wait for beam before going to no-beam regulation
CxGRAD The readback on the tank gradient
LxGADJ The setpoint for the gradient
KxLPGN The gain on the loop. This number is between +0.1 and +0.5

The startup parameters are:
Avgcyc How many cycles to average the beam-on information (32)
Loadcyc How many cycles to average the beam-off cycles (128)

The LA looks at the cavity gradient on every cycle and calculates a new setpoint based on (1) how far off the reading is from where is should be (2) the value of the gain and (3) the value of the setpoint (it will not make a setting so that LxGADJ goes out of tolerance). If this was a beam pulse, it adjusts the gradient to the nominal value. If it is not a beam pulse, then it calculates the "beam loading" so that when it starts regulating without beam, it knows how to set the gradient.

You stop learning by turning off the loop entirely.

More info available upon request.

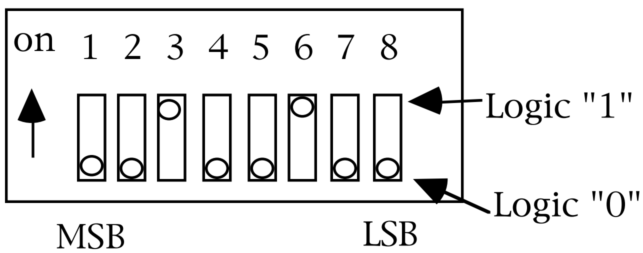
Elliott.

Appendix III: Module Switch Settings

There are 8 contact dip switches on the Phase Detector/Shifter Module and the LLRF Module. These determine the Logical Device number for proper addressing to the computer. Proper device number = Slot number x 4. The multiplier of 4 was used so that more than 12 slot functions could be addressed.

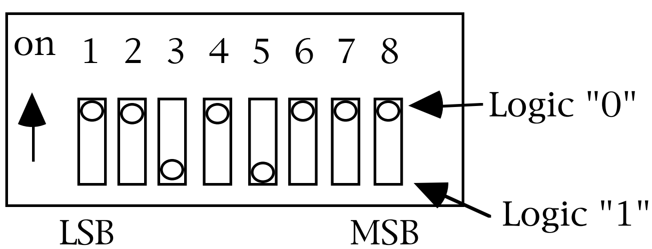
NOTE: the switches are different between the two different cards as shown below!!

LLRF Module:



This switch is set for Slot 9, logical device 36.

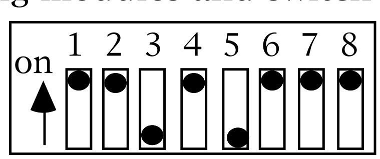
Phase Detector/Shifter Module:



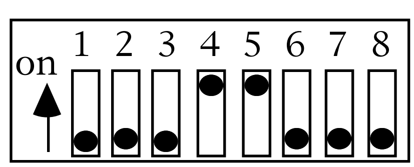
This switch is set for slot #5, logical device 20.

The transition section has the following modules and switch settings:

Slot #5: Phase Det/Sh.



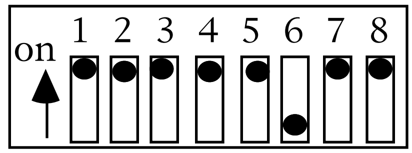
Slot #6: LLRF



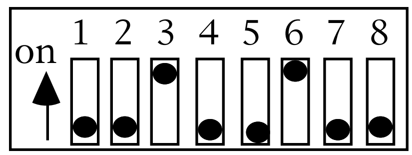
Appendix III: Module Switch Settings continued

Transition section continued

Slot #8: Phase Det/Sh.

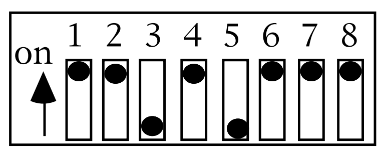


Slot #9: LLRF

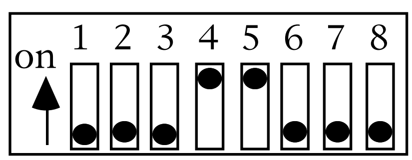


Stations 1-7 and debuncher have the following modules and switch settings:

Slot #5: Phase Det/Sh.

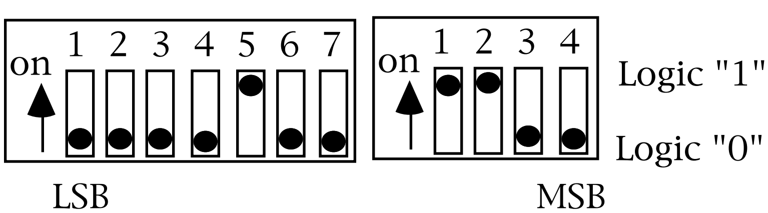


Slot #6: LLRF



Phase/VCXO:

Phase Sample Delay



The phase is sampled at 100ns x switch setting after the LLRF trigger. For example this switch is set to 40 us.

Appendix IV: Schematics

Appendix V: System Calibrations

Appendix VI: Memory map

LINAC Upgrade Low Level RF
805 Mhz Phase Detector/Shifter Module

Memory Map for Data Access

1st Station in Crate		Memory Location
LxSDLY	PH360 ADC DELAY	41889ABA
CxPADJ	PH360 PH SET DAC	41889ABC
LxSTMP	PH360 OVEN TEMP	41889ABE
LxSDET	PH360 DIODE DET	41889AC0
LxSIPH	PH360 I PHASE	41889AC2
LxSQPH	PH360 Q PHASE	41889AC4

2nd Station in Crate

LxSDLY	PH360 ADC DELAY	418a3d74
CxPADJ	PH360 PH SET DAC	418a3d76
LxSTMP	PH360 OVEN TEMP	418a3d78
LxSDET	PH360 DIODE DET	418a3d7a
LxSIPH	PH360 I PHASE	418a3d7c
LxSQPH	PH360 Q PHASE	418a3d7e

For test that writes to DAC and reads from corresponding ADC
(ie DAC is connected to ADC for test):

dac_adc_test WRITE is at $00846000

dac_adc_test READ is at $00847000

The base address of (STATION 0) madc_test_result is $00852000

result: $00852000
readings: $00854000

result: $00856000
readings: $00858000

result: $0085A000
readings: $0085C000

The base address of (STATION 1) madc_test_result is $0085E000

result: $0085E000
readings: $00860000

result: $00862000
readings: $00864000

result: $00866000
readings: $00868000

Madc_test_result data goes to $0086A000

The base address of (STATION 0) fifo_result is $0086A000

result: $0086A000

The base address of (STATION 1) fifo_result is $0086C000

result: $0086C000

Fifo_result data goes to $0086E000

The base address of (STATION 0) real-time data is $00870000
Phase data:
-head: $00870000
-tail: $00870004
-waveform: $00870008
-t0: $0087C35A
-n0: $0087C35E
-t1: $0087C362

-n1: $0087C366
-t2: $0087C36A
-n2: $0087C36E
-integrator: $0087C370
-n: $0087C374
-ff_wave: $0087B008
-gain: $0087CD3E
-offset: $0087CD42

Magnitude data:
-head: $0087CD44
-tail: $0087CD48
-waveform: $0087CD4C
-t0: $0088909E
-n0: $008890A2
-t1: $008890A6
-n1: $008890AA
-t2: $008890AE
-n2: $008890B2
-integrator: $008890B4
-n: $008890B8
-ff_wave: $00887D4C
-gain: $00889A82
-offset: $00889A86

madc_data: $00889A88
misc_status: $00889AA8
misc_control: $00889AAA
magnitude_nom: $00889AAC
phase_offs: $00889AAE
phase_openloop_set_point: $00889AB0
temp_sample_delay: $00889AB2
madc_sample_delay: $00889AB4
fifo_sample_depth: $00889AB6
feedforward_off: $00889AB8
phase360_delay: $00889ABA
phase360_set: $00889ABC
phase360_data: $00889ABE

spare: $00889AC6

The base address of (STATION 1) real-time data is $0088A2BA

Phase data:
-head: $0088A2BA

-tail: $0088A2BE
-waveform: $0088A2C2
-t0: $00896614
-n0: $00896618
-t1: $0089661C
-n1: $00896620
-t2: $00896624
-n2: $00896628
-integrator: $0089662A
-n: $0089662E
-ff_wave: $008952C2
-gain: $00896FF8
-offset: $00896FFC
Magnitude data:
-head: $00896FFE
-tail: $00897002
-waveform: $00897006
-t0: $008A3358
-n0: $008A335C
-t1: $008A3360
-n1: $008A3364
-t2: $008A3368
-n2: $008A336C
-integrator: $008A336E
-n: $008A3372
-ff_wave: $008A2006
-gain: $008A3D3C
-offset: $008A3D40
madc_data: $008A3D42
misc_status: $008A3D62
misc_control: $008A3D64
magnitude_nom: $008A3D66
phase_offs: $008A3D68
phase_openloop_set_point: $008A3D6A
temp_sample_delay: $008A3D6C
madc_sample_delay: $008A3D6E
fifo_sample_depth: $008A3D70
feedforward_off: $008A3D72
phase360_delay: $008A3D74
phase360_set: $008A3D76
phase360_data: $008A3D78

spare: $008A3D80

Real-time data goes to $008A4574

The base address of (STATION 0) diagnostics data is $00850000

Diagnostics data:
do_it: $00850000
=1 to start. Do only after CHOICE filled
choice: $00850002
Fill this 1st. =0 means do all diags
=1 means do fifotest for CHAN
if_pass_all_tests: $00850004
fifo_summary: $00850006
being_done: $0085000A
heartbeat: $0085000C
dac_adc_mode: $00850010
dac_adc_old: $00850012
for_future: $00850014
version: $00850028
fifo_inprg: $00850038
slot: $0085003A
chan: $0085003C
fifo_depth: $0085003E
madc_other[00]: $00850040 Board temperature
result: $00850040
reading: $00850042
expval: $00850044
tol: $00850046
madc_other[01]: $00850048 Magnitude feedforward DAC
result: $00850048
reading: $0085004A
expval: $0085004C
tol: $0085004E
madc_other[02]: $00850050 Phase feedforward DAC
result: $00850050
reading: $00850052
expval: $00850054
tol: $00850056
madc_other[03]: $00850058 Phase detector
result: $00850058
reading: $0085005A

expval: $0085005C
tol: $0085005E
madc_other[04]: $00850060 Phase error
result: $00850060
reading: $00850062
expval: $00850064
tol: $00850066
madc_other[05]: $00850068 Spare
result: $00850068
reading: $0085006A
expval: $0085006C
tol: $0085006E

MADC data[00]: Choice = 2 =
Phase_openloop_setpoint_DAC
overall_result: $00850070
gain: $00850072
offset: $00850076
madc_nom:
off $0085007A
tol_off $0085007E
gain $00850082
tol_gain $00850086
tol: $0085008A
xsum: $0085008E
ysum: $00850092
xysum: $00850096
xsqsum: $0085009A

MADC data[01]: Choice = 3 = Phase offset
overall_result: $0085009E
gain: $008500A0
offset: $008500A4
madc_nom:
off $008500A8
tol_off $008500AC
gain $008500B0
tol_gain $008500B4
tol: $008500B8
xsum: $008500BC
ysum: $008500C0
xysum: $008500C4
xsqsum: $008500C8

MADC data[02]: Choice = 4 = Magnitude nominal
overall_result: $008500CC
gain: $008500CE
offset: $008500D2
madc_nom:
    off $008500D6
    tol_off $008500DA
    gain $008500DE
    tol_gain $008500E2
tol: $008500E6
xsum: $008500EA
ysum: $008500EE
xysum: $008500F2
xsqsum: $008500F6

The base address of (STATION 1) diagnostics data is $008500FA
Diagnostics data:
do_it: $008500FA
    =1 to start. Do only after CHOICE filled
choice: $008500FC
    Fill this 1st. =0 means do all diags
        =1 means do fifotest for CHAN
if_pass_all_tests: $008500FE
fifo_summary: $00850100
being_done: $00850104
heartbeat: $00850106
dac_adc_mode: $0085010A
dac_adc_old: $0085010C
for_future: $0085010E
version: $00850122
fifo_inprg: $00850132
slot: $00850134
chan: $00850136
fifo_depth: $00850138
madc_other[00]: $0085013A Board temperature
    result: $0085013A
    reading: $0085013C
    expval: $0085013E
    tol: $00850140
madc_other[01]: $00850142 Magnitude feedforward DAC

result: $00850142
reading: $00850144
expval: $00850146
tol: $00850148
madc_other[02]: $0085014A Phase feedforward DAC
result: $0085014A
reading: $0085014C
expval: $0085014E
tol: $00850150
madc_other[03]: $00850152 Phase detector
result: $00850152
reading: $00850154
expval: $00850156
tol: $00850158
madc_other[04]: $0085015A Phase error
result: $0085015A
reading: $0085015C
expval: $0085015E
tol: $00850160
madc_other[05]: $00850162 Spare
result: $00850162
reading: $00850164
expval: $00850166
tol: $00850168

MADC data[00]: Choice = 2 =
Phase_openloop_setpoint_DAC
overall_result: $0085016A
gain: $0085016C
offset: $00850170
madc_nom:
off $00850174
tol_off $00850178
gain $0085017C
tol_gain $00850180
tol: $00850184
xsum: $00850188
ysum: $0085018C
xysum: $00850190
xsqsum: $00850194

MADC data[01]: Choice = 3 = Phase offset
overall_result: $00850198

gain: $0085019A
offset: $0085019E
madc_nom:
    off $008501A2
    tol_off $008501A6
    gain $008501AA
    tol_gain $008501AE
tol: $008501B2
xsum: $008501B6
ysum: $008501BA
xysum: $008501BE
xsqsum: $008501C2

MADC data[02]: Choice = 4 = Magnitude nominal
overall_result: $008501C6
gain: $008501C8
offset: $008501CC
madc_nom:
    off $008501D0
    tol_off $008501D4
    gain $008501D8
    tol_gain $008501DC
tol: $008501E0
xsum: $008501E4
ysum: $008501E8
xysum: $008501EC
xsqsum: $008501F0

Diagnostics data goes to $008501F4

%SYSTEM-F-ACCVIO, access violation, reason mask=00, virtual address=00000000, PC=00000000, PSL=03C00000
%TRACE-I-BADDST, no symbols in image
%TRACE-F-STACKDUMP, non-symbolic stack dump follows

module name	routine name	line	rel PC	abs PC
			00000000	00000000

BEC 9/15/93

LLRF INTERFACE CARD REGISTER DEFINITION

Control Register

Bit #	
15	NC
14	NC
13	NC
12	NC
11	NC
10	NC
9	Trigger Enable
8	Interrupt level bit 3
7	Interrupt level bit 2
6	Interrupt level bit 1
5	Start digitize
4	Interrupt mode
3	Reset fifo memory address
2	NC
1	System fault inhibit
0	Reset

Status Register

Bit #	
15	A24/A32
14	nMod ID
13	0
12	0
11	Interrupt Request
10	Hold mode for S/H
9	TRIGGER ENABLE
8	Interrupt bit 3
7	Interrupt bit 2
6	interrupt bit 1
5	Digitization in progress
4	Interrupt mode
3	Ready

2	Passed
1	System fault inhibit
0	Reset

Board Control Register

Bit#	
7	
6	VCXO board spare
5	VCXO enable
4	RF output disable
3	Magnitude loop disable
2	Phase Flip
1	Phase loop disable
0	Test mode D/A feedback to A/D

Board Status Register

Bit#	
15	NC
14	DA to AD
13	NC
12	VCXO Vin switch status
11	VCXO RF switch status
10	NC
9	NC
8	Beam Present
7	Phase Flip FP *
6	RF enable FP *
5	NC
4	Magnitude loop enable*
3	Phase "-" *
2	Phase "+" *
1	Phase loop enable*
0	Mixer #1 enable*

LINAC UPGRADE
LOW LEVEL RF MODULE
PROGRAMMERS MODEL
12/20/91

ADDRESS OFFSET	Channel	
3E	MADC 16	Phase Shifter
3C	MADC 15	Phase Error
3A	MADC 14	Phase Feedforward DAC
38	MADC 13	Phase Detector
36	MADC 12	Mag Mixer Drive
34	MADC 11	Magnitude Error
32	MADC 10	Magnitude Feedforward DAC
30	MADC 9	Magnitude Detector
2E	MADC 8	Magnitude set DAC
2C	MADC 7	Local Bus 01
2A	MADC 6	Local Bus 02
28	MADC 5	Local Bus 03
26	MADC 4	Board Temperture
24	MADC 3	Phase Open Loop set DAC
22	MADC 2	Phase Offset set DAC
20	MADC 1	Local Bus 00
1E	Board Status	
1C	Board Control	
1A	Magnitude Nominal DAC 12 Bit	
18	Phase Offset Set DAC 12 Bit	
16	Magnitude DAC 12 Bit (fast)	
14	Magnitude ADC 8 Bit (fast)	
12	Phase DAC 12 Bit (fast)	
10	Phase ADC 8 Bit (fast)	
0E	Phase Open Loop Set DAC 12 Bit	
0C	Temp Loop Delay 11Bit	
0A	MADC Delay 11 Bit	
08	Fifo Depth 11 Bit	
06	Offset Register	
04	Status/Control Register	
02	Device Type (AAAA)	
00	ID Register (4321)	

Address = FFFFC000h + (40h * Device#) + Offset